SARFRAZ HUSSAIN

PhD & M.Tech (Mixed Signal Circuit Design) NERIST, Arunachal Pradesh, India
CDC Lab, Indian Institute of Technology (IIT), Guwahati, Assam, India
(*Visvesvaraya PhD Fellow, Ministry of Electronics and IT (MeitY), Govt. of India*)
Young Researcher Award, IEI & REST Labs India
UGC National Eligibility Test (NET) Qualified, India
NPTEL STAR Domain Certificate in Electrical Engineering (VLSI Design)
Mandarin Language Certification at Shou University, Taiwan
Webpage : **https://sites.google.com/view/sarfrazhussain/home**
LinkedIn page : **https://www.linkedin.com/in/dr-sarfraz-hussain-21b72118/**

Expertise in Analog and Mixed Signal IC Design, IoT and Embedded System
Mandarin Language Certification Scholarship by Taiwan Embassy at I-Shou University, Taiwan
Total Experience: Research 5 yrs, pre-PhD 1 yr 5 mnths, post-PhD 3 yrs

CAREER OBJECTIVE

Highly motivated and dedicated professional seeking a challenging position in the field of IC Design and Fabrication. Motivated to work in an environment that gives me ample opportunities to harness knowledge and enhance it further. I want to utilize my knowledge, experience, and skills to contribute significantly to the development of scientific research activities and growth of the organization. **Experience in ASIC design flow**.

CAREER HIGHLIGHTS

- More than 8 years of research experience in IC design and VLSI Technology.

- NPTEL Domain Certificate in Electrical Engineering (VLSI Design)

- Visvesvaraya PhD Fellow, funded by Ministry of Electronics and IT (MeitY), Govt. of India.

- TEQIP fellowship for M.Tech in VLSI, NERIST, Arunachal Pradesh, India.

- UGC-National Eligibility Test for Assistant Professor in Electronics Science (Qualified in 2018).

- Best Paper Presentation Award in IEEE Conference (IACIS-2024).

- IEEE Senior Member, ISTE Life Member.

- Secretary, IEEE SA Workgroup on Child Safety and AI (P3462) (2024 to present).

- Secretary IEEE Circuits and Systems Society (CASS), Execom CEDA (2025)

- Execom IEEE CS, CEDA, Secretary Systems Council (2024).

- Received scholarship for 3 months for Language Certification in Mandarin at Taiwan Shou University.

- Publications: Journals-4, Book-1, Book Chapter-3, Conferences-8

- Guidance: PhD - 1; MTech - 2; BTech - 10 Groups

AREA OF INTEREST (VLSI IC Design & Fabrication)

Analog IC Design & Layout	Flexible & Wearable Electronics
Digital IC Design & Layout	IoT & Healthcare

SKILLS & EXPERTISE

- **ASIC Design Knowledge:**
  Understanding of Circuit level design and Simulation. PVT Analysis, Corner Analysis, Monte Carlo Analysis. Post-Layout Simulation, DRC, LVS, ERC.

- **Software skills (Professional):**
  Languages (C), **Script** (Python: Matplotlib, numpy, pandas), **Tools** (LaTeX, Jupyter notebook, **MATLAB:** Code editor, Simulink, GUI, **CADENCE Virtuoso:** from simulation to post layout, **ngSpice, LTSpice, HSpice, Tanner tools, Electric VLSI, Chisel−chip development tool, Xilinx**).

- **Soft skills:**
  Skilled in adapting to and thriving in multidisciplinary work environments, problem solving, work ethic, quick learner, self-motivated, technical writing skills, strong communication skills, and hard working.

- **Teaching Experience:**
  Post-PhD Teaching Experience: >2 years. **Total Teaching Experience:** 4 Years **During PhD:** 5 Years.
  Subjects: Analog Electronics, Linear Integrated Circuits, Digital Electronics, IoT, Embedded System.
  Courses: B.Tech and M.Tech. **M.Tech Project Guided:** 1, Guiding 1; **PhD Guiding**: 1.

STRONG RESEARCH COLLABORATIONS

- **H. S. Jatana**, Head of Design Team (former), **Semiconductor Lab (SCL)**, Mohali (*Fabrication and Manufacturing*) now under **ISRO, India**.

- **Prof. Dr. Gaurav Trivedi**, **Indian Institute of Technology (IIT), Guwahati, India**.

PROFFESSIONAL TRAININGS ATTENDED

- **Embedded Systems (8051 micro-controller)**
  1st Jan to 14th Jan 2009
  (CETPA INFOTECH PVT. LTD, Greater Noida, U.P.)

- **Internship on Custom IC Design: CMOS Standard Cell Circuit Design, Simulation And Layout**
  8th July to 4th September 2020
  (Entuple Technologies, Online)

FELLOWSHIP & ACHIEVEMENTS

- **NPTEL STARS** for Domain Certification in VLSI Design and Discipline Certification in Electrical Engineering (Dec. 2024).

- **Young Researcher Award** awarded at International Conference on Science and Engineering organized by REST Labs & IEI, Hosur Local Centre at REST Labs, REST Campus, Kaveripattinam, Krishnagiri, Tamil Nadu, India on 27 February **(2023)**.

- **Visvesvaraya Ph.D. Scholar**: Visvesvaraya Ph.D. Scheme under *Ministry of Electronics and Information Technology* (**Meity**), Govt. of India, implemented by *Digital India Corporation* (**DIC**). (**Grant:** PhD-MLA-4(96)/2015-2016, **unique awardee ID:** VISPHD-MEITY-1864) (**2015**)

- **UGC-National Eligibility Test (NET)**: Year- **2017**, Qualified for *Assistant Professor*, Marks-**230**, Percentage-**65.71%**

- **IEEEXTREME Ambassador and Proctor** for *Programming Competition* (**2023, 2024**)

- **Third** position is *Zonal Robotics competition* (**2010**)

- Awarded with **Role of Honour** by the school for *only student* in school to get *distinction* in all the subjects. *Class X*, CBSE board, **2004**.

RESEARCH Links

- LinkedIn page : **https://www.linkedin.com/in/dr-sarfraz-hussain-21b72118/**

- ORCID : **https://orcid.org/0000-0002-2585-1122**

- Google Scholar page : **https://scholar.google.co.in/citations?user=H5j6OMoAAAAJ&hl=en**

- Scopus page : **https://www.scopus.com/authid/detail.uri?authorId=57210529222**

ACADEMICS

Examination/ Degree	Board/ University	School/ Institute	Duration of Course	CGPA/ %
PhD in *Electronics and Communication Engineering (ECE)*	NERIST *(Arunachal Pradesh)*	NERIST *(Arunachal Pradesh)*	2015-2021	9/10 85.00
M.Tech in *Very Large Scale Integration (VLSI)*	NERIST *(Arunachal Pradesh)*	NERIST *(Arunachal Pradesh)*	2012-2014	4.25/5 76.00
B.Tech in *Electronics and Communication Engineering (ECE)*	NEHU *(Meghalaya)*	NEHU *(Meghalaya)*	2006-2010	6.1/9 66.00
Class XII *AISSCE*	CBSE	K. V. No.1, Itanagar *(Arunachal Pradesh)*	2005-2006	70.00
Class X *AISSE*	CBSE	Govt. Hr. Sec. School, *Naharlagun*, *(Arunachal Pradesh)*	2003-2004	83.40

Note: Ph.D. Awarded provisionally on 16-02-2021; Thesis submitted on 31-08-2020; defended on 15-01-2021

NERIST: **N**orth **E**astern **R**egional **I**nstitute of **S**cience and **T**echnology (*Deemed to be University, CFTI*)
NEHU: **N**orth **E**astern **H**ill **U**niversity (*Central University*)
CBSE: **C**entral **B**oard of **S**econdary **E**ducation

TEACHING EXPERIENCE

Post held	Regular/Temporary	Organization	Tenure
Assistant Professor *School of ECE*	Regular	REVA University *(Karnataka)*	03/07/2023 to present *(1 year 8 months)*
Assistant Professor *Dept. of ECE*	Regular	MITS *(Andhra Pradesh)*	24/12/2021 to 27/06/2023 *(1 year 6 months)*
Assistant Professor *Dept. of ECE*	Contractual	NERIST *(Arunachal Pradesh)*	16/01/2015 to 31/05/2015 *(5 Months)*
Guest Lecturer *Dept. of ECE*	Temporary	NERIST *(Arunachal Pradesh)*	20/07/2011 to 31/05/2012 *(11 Months)*

PROFESSIONAL MEMBERSHIP & PARTICIPATION

- **IEEE Senior Member** and **ISTE Life Member**.

- **Secretary IEEE Circuits & Systems Society** and Execom **IEEE CEDA** (2025).

- **Secretary IEEE Systems Council** Bangalore Chapter R-10 (2024).

- **Execom IEEE CEDA** and **Computer Society** Bangalore Chapter R-10 (2024).

- **Member** of Workgroup **IEEE SA Flexible & Wearable Electronics CASS**

- **Secretary IEEE P3462 Workgroup:** Recommended Practice for Using Safety by Design in Generative Models to Prioritize Child Safety sponsored by Artificial Intelligence Standards Committee

- **Advisory Board Member** of **Generation of Thinkers (GoT)**

- **Reviewer**, **Session Chair**, **TPC member and Co-Chair** in several IEEE Conferences like **ISCAS, APPCAS, VLSI SATA**, etc.

- **Academic Liaison Chair** for **SWEAT 2024 (IEEE CEDA Bangalore Chapter R-10)**.

- **Steering Committee Member Girl Geek 2024** (IEEE Computer Society Bangalore Chapter R-10).

- **Speaker and Resource person** for **AICTE Training and Learning (ATAL) Faculty Development Programme (FDP), Joint EICT FDP funded by MeitY, Govt of India** and other Skill Development Events.

- **Committee Member & Speaker** in IEEE CEDA event **FAB.ulous**.

- **Mentor** for **IEEE CS and CASS**.

PROJECTS

- **DESIGN OF AN EFFICIENT ADC FOR LOW-POWER AND HIGH-SPEED APPLICATIONS**
  (Ph.D. Research Project)(*July, 2015 - January, 2021*)

  Supervisor: Dr. Rajesh Kumar, ECE Deptt., NERIST, Arunachal Pradesh,
  Co-Supervisor: Dr. Gaurav Trivedi, EEE Deptt., IIT Guwahati, Assam.
    - **Objective :** Performance improvement of Flash ADC in terms of low-power dissipation, higher speed, high resolution, bubble error correction, and application-independent implementation.
    - **Brief Description :** Analog-to-digital converter (ADC) is the intermediate connector between the analog and digital worlds. Flash ADC is the fastest ADC. An efficient ADC reduces power dissipation in mixed signal systems and therefore, increases performance. The bubble error corrector is designed to overcome the bubble error problem and increases the effective number of bits (ENOB). A resolution-selective approach makes the proposed design application independent and saves manufacturing costs. Simulations were carried out in *CADENCE design environment (Virtuoso)* and layout was made using *CADENCE layout editor*. *Spectre* simulator was used to carry out the analysis. *MATLAB* was used to plot the output and comparison graphs. *PYTHON* programming language is to verify and implement the proposed algorithm.
    - **Software used :** CADENCE EDA tools, MATLAB, Jupyter notebook (Python)
    - **Application :** Flash ADCs can be used in optical communication, wideband communication, image sensing, CD-ROM R/W, etc.

- **8-BIT 1-GSPS FLASH ADC FOR OPTICAL COMMUNICATION RECEIVERS**
  (M.Tech Project)(*July, 2013 - May, 2014*)

  Supervisor: Mr. Ashok Kumar Ray, ECE Deptt., NERIST, Arunachal Pradesh
    - **Objective :** To design an 8-bit Flash ADC that can process 1-Giga samples per second.
    - **Brief Description :** The encoder with a bubble error corrector is designed to reduce the overall power dissipation and to increase the speed of ADC as a whole. Bubble error up to an order of 2 is corrected by using the proposed design. Simulations were carried out in *CADENCE design environment (Virtuoso)* and layout was made using *CADENCE layout editor*. *Spectre* simulator was used to carry out the analysis. *MATLAB* was used to plot the output and comparison graphs.
    - **Software used :** CADENCE EDA tools, MATLAB
    - **Application :** Proposed flash ADCs are designed for optical communication applications.

- **AUTOMATIC MONITOR AND CONTROL OF GREENHOUSE ENVIRONMENT USING MICRO-CONTROLLERS**
  (B.Tech Major Project)(*January, 2010 - July, 2010*)

  Supervisor: Dr. Rajkishur Mudoi, ECE Deptt., NEHU, Meghalaya
    - **Objective :** To automatically monitor as well as control the greenhouse environment.
    - **Brief Description :** 8051 microcontroller kit (easy 8051b) was used to show the feasibility of the project. The values were shown in a 2×16 line LCD with continuous temperature monitoring and other parameters. If the temperature rises above the allowable temperature then the fan is switched on and the temperature is automatically lowered. Similarly, if the sunlight is low, then according to the reading of a LDR bulbs are switched on to maintain the light for the healthy growth of the plants. MICRO C language was used in this project. The kit used, has many other functionalities so we can use many other sensors to interface with the microcontroller. Even other ADCs or DACs can also be connected.
    - **Software used :** Micro C language based development software.
    - **Hardware used :** Easy 8051b microcontroller kit, temperature sensor, ADC, LCD, LDR, Fan, Stepper Motor, LEDs, Buzzer.

- ○ **Application :** It is applied to greenhouses and can be used by farmers to grow plants in a controlled environment.

- **A PROTOTYPE OF METRO TRAIN**
  (Training Project)(*January, 2010 - January, 2010*)

  Trainer: CETPA PVT Infotech, Greater Noida, Uttar Pradesh
  - ○ **Objective :** To design and simulate a prototype of the Metro Train.
  - ○ **Brief Description :** It includes the interfacing of LCD, Stepper motor, Buzzer, and LEDs with the 8051 microcontrollers. When the train moves from STATION A to STATION B the STATION NAME is displayed on the LCD. The stepper motor is responsible for the movement of the train, and the start and stop times can be fixed by programming the microcontroller. During an emergency, the LED turns ON and the buzzer is also set and an interrupt stops the train. This is a prototype of the Metro Train. Furthermore, a temperature sensor can also be interfaced to show the temperature inside the compartment.
  - ○ **Software used :** Embedded 8051 assembly language-based development software.
  - ○ **Hardware used :** 8051 Microcontroller PCB, LCD, Stepper Motor, LEDs, Buzzer.
  - ○ **Application :** It can be used in Metro trains and Smart Buses.

- **FACE DETECTION USING NEURAL NETWORKS**
  (B.Tech Minor Project)(*January, 2008 - July, 2008*)

  Supervisor: Dr. Rajkishur Mudoi, ECE Deptt., NEHU, Meghalaya
  - ○ **Objective :** To detect the faces using neural networks.
  - ○ **Brief Description :** MATLAB was used for simulation purpose. The neural network is trained again and again with different images of faces to show better output. A database of different faces is created first, then an input image is processed using MATLAB, and faces are detected using the algorithm. The process of segmentation is followed so as to identify the color pigment of our skin. So segmentation is done using many different faces. The more faces the more accuracy we will get.
  - ○ **Software used :** MATLAB
  - ○ **Application :** Face detection applications like surveillance.

PUBLICATION IN REPUTED CONFERENCES, JOURNALS AND BOOKS

- **JOURNALS**

  1. Shailendra Kumar Tripathi, **Sarfraz Hussain**, Raj Kumar, Sourabh Sahu, "**Design and Analysis of Digitally Tunable Transconductance Amplifier (DTTA) Using CNTFETs**", *The Scientific World Journal*, vol. 2024, Article ID 2003437, 6 pages, 2024.**DOI:** 10.1155/2024/2003437. Published on 23 May 2024 (Q2, Scopus Indexed, Impact factor 1.219)

  2. **S. Hussain**, "**Resolution-Selective and Resolution-Adaptive 2 to 8-bit Flash ADC for High-Speed Application Independent IC (HS-AIIC)**", *Journal of Circuits, Systems, and Computers*, Volume- 31 No. 09, Pages- 1-23, June *2022*. **DOI:** 10.1142/S0218126622501699. Online ready 24th March 2022 (SCI Indexed, Impact factor 1.33)

  3. **S. Hussain**, R. Kumar and G. Trivedi, "**Methodology and Comparative design of an efficient 4-bit Encoder with bubble error corrector for 1-GSPS Flash type ADC**", *IET Circuits, Devices & Systems*, Vol. 14, Iss. 5, pp. 629-639, August *2020*. **DOI:** 10.1049/iet-cds.2019.0499 (SCI Indexed, Impact factor 1.29)

- **BOOKS/BOOK CHAPTER**

  1. B. Nadeem, N. Hothi, R. Malik, J. Gupta, and **S. Hussain**, "**Temporal Variations of Sulfur Dioxide Levels across India**", *Artificial Intelligence for Air Quality Monitoring and Prediction. CRC Press, Taylor & Francis Group.*, Chapter-2, Vol.1 , pp. 24-38. August. *2024*. eBook ISBN: 9781032683805. Editors: Amit Awasthi, Kanhu Charan Pattnayak, Gaurav Dhiman, Pushp Raj Tiwari. **DOI:** 10.1201/9781032683805 (Scopus Indexed)

  2. **S. Hussain**, and A. K. Shaw, "**Future of Internet of Nano Things (IoNT) in India**", *In: Fong, S., Dey, N., Joshi, A. (eds) ICT Analysis and Applications. ICT4SD 2024. Lecture Notes in Networks and Systems (LNNS)*, vol 1162. pp 537–544 Springer, Singapore (Scopus Indexed) e-ISBN: 978-981-97-8605-3. *2024*. Springer, Singapore. (Scopus Indexed) Online: 14 November 2024. **DOI:** 10.1007/978-981-97-8605-3_48

  3. Pramod Sharma, Ashwini A. Ankar, **Sarfraz Hussain**, and R. Remya, "**Wireless Networks**", Dec. *2023*. REST Publishers, India. **ISBN** 978-81-967689-8-0

4. **S. Hussain**, R. Kumar and G. Trivedi, "**Resolution Selective 2 to 6 - bit Flash ADC in 45nm Technology**", *Electronic Systems and Intelligent Computing (ESIC). Lecture Notes in Electrical Engineering (LNEE)*, Vol. 686, pp. 475-483. Sept. *2020*. Springer, Singapore. Editors: P. K. Mallick, P. Meher, A. Majumder, S. K. Das.. **DOI:** 10.1007/978-981-15-7031-5_45 (Scopus Indexed)

- **CONFERENCES**

    1. Abhilash, and **S. Hussain**, "**Comparative Analysis of Parallel Prefix Adders**", *2024 IEEE International Conference on Intelligent Algorithms for Computational Intelligence Systems (IACIS-2024)*, pp. , Navkis College of Engineering, Hassan, Karnataka, India, 23-24 August. *2024. DOI: 10.1109/IACIS61494.2024.10721962, BEST PAPER PRESENTER AWARD* 24 October 2024 added to IEEE Xplore

    2. **S. Hussain**, Sandeep A, Chakradhar Sai Meruva and Kiran Panchal, "**Early Detection of Sleep Apnea by Non-Invasive Method : A Review**", *2024 IEEE International Conference on Recent Innovation in Smart and Sustainable Technology (ICRISST 2024)*, pp. , Bengaluru, Karnataka, India, March. *2024.* **DOI:** 10.1109/ICRISST59181.2024.10921832 20th March 2025 added to IEEE Xplore.

    3. **S. Hussain** and S. Deb, "**A Study on Securing Data in Smart Healthcare Applications**", *7th IEEE International Symposium on Smart Electronic Systems (IEEE − iSES, formerly IEEE − iNIS)*, pp. 343-348, Jaipur, Rajasthan, India, Dec. *2021.* **DOI:** 10.1109/iSES52644.2021.00087

    4. **S. Hussain**, R. Kumar, and G. Trivedi, "**Comparison of NMOS and PMOS Input Driving Dynamic Comparator in 45nm Technology**", Proceedings of the 6th International Conference on Computers, Management & Mathematical Sciences (ICCM 2020), NERIST, Nirjuli, Arunachal Pradesh, India. 22-23 Dec. *2020*, Vol. 1020, Issue 012022, pp- 1-7. IOP Conference Series: Materials Science and Engineering. **DOI:** 10.1088/1757-899x/1020/1/012022. IOP Publishing Ltd. (Scopus indexed) Online ISSN: 1757-899X Print ISSN: 1757-8981

    5. **S. Hussain** and R. Kumar, "**Design of a Low Power and High Speed Wallace Tree Encoder for Flash ADC**", *Proceedings of the 5th International Conference on Computers & Management Skills (ICCM 2019)*, pp. 34-39, Nirjuli, Arunachal Pradesh, India, Jan. *2020.* **DOI:** 10.2139/ssrn.3516639

    6. **S. Hussain**, R. Kumar and G. Trivedi, "**Comparison and Design of Dynamic Comparator in 180nm SCL Technology for Low Power and High-Speed Flash ADC**", 2017 *IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pp. 139-144, Bhopal, MP, India, Dec. *2017*. **DOI:** 10.1109/iNIS.2017.37 (Scopus Indexed) (Under top 50 most read conference paper of iNIS)

    7. **S. Hussain**, R. Kumar and G. Trivedi, "**A Novel Low Power High-Speed BEC for 2GHz Sampling Rate Flash ADC in 45nm Technology**", *2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pp. 133-138, Bhopal, MP, India, Dec. *2017*. **DOI:** 10.1109/iNIS.2017.36 (Scopus Indexed)

    8. **S. Hussain** and M. Kumar, "**Design of an efficient 8-bit flash ADC for optical communication receivers**", 2016 *International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, pp. 449-453, Chennai, TN, India, March *2016*. **DOI:** 10.1109/ICEEOT.2016.7755560 (Scopus Indexed)

WORKSHOPS, SEMINARS AND SHORT-TERM COURSES

- **National Programme on Technology Enhanced Learning (NPTEL) Certifications**

    ○ FDP and NPTEL Certification in Microprocessors And Interfacing(*Registered*), 12-weeks, **2024** (Online).
    ○ FDP and NPTEL Certification in Analog Circuits(*Exam Concluded*), 8-weeks, **2024** (Online).
    ○ NPTEL Certification in Python for Data Science (Elite), 4-weeks, **2023** (Online).
    ○ FDP and NPTEL Certification in Digital Electronic Circuits(Elite + Silver), 12-weeks, **2023** (Online).
    ○ FDP and NPTEL Certification in System Design Through VERILOG(Elite + Silver), 8-weeks, **2022** (Online).
    ○ FDP and NPTEL Certification in CMOS Digital VLSI Design(Elite + Silver), 8-weeks, **2022** (Online).

- **WORKSHOPS**

    ○ **Organized** a 5-day workshop on "*The Art of Patenting and Drafting*" from 25-29 April **2022** (Online). MITS, Andhra Pradesh.
    ○ **IP Awareness/Training program** under *National Intellectual Property Awareness Mission* organized by Intellectual Property Office, India (GOI Initiative) on May 03,2024
    ○ Two days IEEE sponsored workshop on Advanced Photonics in the Centre for Advanced Electronics, 30 Nov. - 1 Dec. **2022**. (IIT Indore)
    ○ One day Industry Oriented Workshop on Recent Trends and Research Perspectives on VLSI and Power Electronics, 4 Oct. **2022**. (Online mode). (School of Electronics Engineering (SENSE), VIT-AP University, Amaravati)

- Five days Workshop on The Art of Patenting and Drafting (Online mode), 25-29 April **2022**, MITS, Madanapalle, Andhra Pradesh. (Organised and participated)
- Three days Research Evaluation Workshop for Visvesvaraya Ph.D. Scheme for Electronics & Information Technology, 17-19 July **2019**, Punjab Engineering College, Chandigarh. (Digital India Corporation & MeitY, Govt. of India)
- Three days Workshop on Schematic and Layout Design Flow in Cadence, 16-18 Jan **2014**, NIT Meghalaya, India. (Entuple & NIT Meghalaya)
- Two days Workshop on MEMS & Sensors, 11-12 Sept. **2013**, NIT Silchar, Assam, India. (IEEE EDS Student Branch Chapter NIT Silchar)
- Three days Workshop on National Program on Micro and Smart Systems (NPMASS) - Institute of Smart Structures and Systems (ISSS) MEMS, 25 - 27 March **2010**, NEHU, Meghalaya, India. (NESAC Department of Space Govt of India & NEHU)

- **SEMINARS/CONFERENCES/SYMPOSIUMS**

  - **One-day Webinar** on Vector Network Analyser + RF Characterization Equipment Overview by Electronics For You, 17th February **2023**.
  - **One day Seminar** on *Journey Beyond Chip War: Unleashing the Art of Chip Design* organized by Maven Silicon, Bengaluru on 7th Oct. **2023**.
  - **Half-day seminar** on Internet of Bodies for seamless Human-Machine Co-operation and Real-time AI organized by IEEE-IISc VLSI Chapter on Jan. 15, **2024**.
  - **One-day Seminar** on Multi Gate Devices for VLSI Design by Dr. Balwinder Raj of NITTTR, Chandigarh, 20 Dec **2022**, Online Mode. (Organized in association with MITS IEEE Student Branch)
  - One-day Seminar on Nanotechnology & Nanoelectronics delivered by Dr. Navakanta Bhat of IISc Bangalore, 29 March **2010**, Shillong, Meghalaya, India. (Student Forum ECE Department, NEHU)
  - 36th **International** Conference on VLSI Design and 22nd International Conference on Embedded Systems (VLSID2023), 8 - 12 Jan. **2023**, Novotel, HICC, Hyderabad. (VLSI Society of India)
  - 35th **International** Conference on VLSI Design and 21st International Conference on Embedded Systems (VLSID2022), 26 Feb. - 2 March **2022**, through Virtual Mode. (VLSI Society of India)
  - 6th **International** Conference on Computers, Management & Mathematical Sciences (ICCM 2020), 22-23 Nov. **2020**, NERIST, Nirjuli, Arunachal Pradesh, India. (IAASSE & NERIST)
  - 1st **International** Conference on Electronic Systems & Intelligent Computing, 2-4 March **2020**, NITAP, Arunachal Pradesh, India. (Springer & NITAP)
  - 5th **International** Conference on Computers & Management Skills (ICCM 2019), 15-16 Dec. **2019**, NERIST, Nirjuli, Arunachal Pradesh, India. (IAASSE, SSRN, Center for Global Management & NERIST)
  - **International** Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT 2016), 3-5 March **2016**, DMI College of Engineering, Chennai, Tamil Nadu, India. (IEEE Madras Section & DMI)
  - 4th **International** Conference on Recent Trends in Engineering & Technology (ICRTET 2015), 2-4 July **2015**, SNJB's Late Sau. Kantabai Bhavarlalji Jain College of Engineering, Neminagar, Chandwad, Nasik, Maharashtra, India. (McGraw Hill Education, IJMTER & SNJB College of Engg.)
  - **International** Conference on Emerging Trends in Science, Engineering, Business and Disaster Management (ICBDM 2014), 28 Feb. **2014**, Noorul Islam University, Kumaracoil, Tamil Nadu, India. (IEEE Madras Section ED Chapter & ISTE India)
  - **National** Conference on Computing, Communication and Information Processing (NCCCIP 2015), 2-3 May **2015**, NERIST, Arunachal Pradesh, India. (CSI Kolkata Chapter, AICTE-NEQIP & NERIST)
  - **National** Conference on Advances in Welding Technology, 10-11 May **2013**, NERIST, Arunachal Pradesh, India. (TEQIP-II, Indian Welding Society Guwahati & NERIST)
  - 2021 IEEE **International Symposium** on Smart Electronic Systems (iSES), 20-22 Dec **2021**, MNIT Jaipur, India.
  - 3rd IEEE **International Symposium** on Nanoelectronic and Information Systems (iNIS 2017), 18-20 Dec. **2017**, Bhopal, Madhya Pradesh, India. (IEEE Computer Society, TCVLSI, CEDA & Oriental Group of Institutions)

- **FDPs/SHORT-TERM COURSES**

  - **One Week Short-Term Course** on *Advances in Signal Processing, Communication and VLSI Design (ASPCV-2024)* Organized by Department of Electronics & Communication Engineering National Institute of Technology Delhi, from April 22-27, **2024**.
  - Participated as a **Mentee** in Electronics and Communication Engineering Stream under **Professional Mentoring Program** for *Young Faculty Members* organized by IEEE India Council Industry Academia Young Professionals Sub-Committee from 1 Oct. to 31 Dec., **2023**.
  - **ATAL FDP** on *Design Build and Real world usage of Drones*, 8-13 Jan. **2024** (6 Days). (REVA University, Bengaluru, Karnataka)

- **ATAL FDP** on *Threats and Challenges in Cyber Security using Data Analytics and Machine Intelligence*, 18-23 Dec. **2023** (6 Days). (REVA University, Bengaluru, Karnataka)
- **FDP** on *Effect of Generative AI in Modern Research and Industry* organized by dept. of CSE, Sister Nivedita University, Kolkata, India from 29th April to 3rd May **2024** (5 days).
- **FDP** on *Hands-on Analog and Digital IC Design using Cadence Tools*, 10-12 Aug. **2023** (3 days). (REVA University, Bengaluru, Karnataka)
- **FDP** on *Hands-on Training in Control Systems and Data Acquisition Systems using Labview*, 10-12 Aug (3 days). **2023**. (REVA University, Bengaluru, Karnataka)
- **FDP** on *Emerging trends in communication and signal processing for next-generation applications*, 12-16 Sept. **2022**, (Online). (BBIT, Kolkata, WB)
- **FDP** on *Recent Developments on MEMS Actuators* & Sensors, 2-6 May **2022**. (Online). (RGU, Itanagar, Arunachal Pradesh)
- **FDP** on *Emerging Trends in Research Paper Writing*,18-22 April **2022**, (Online). (REST Society for Research International (RSRI) Krishnagiri, Tamil Nadu)
- **FDP** on *VLSI Chip Design Hands-on using Open Source EDA*, 8-12 July **2019**, (Online). (E&ICT Academy IIT Guwahati & NERIST)
- **FDP** on *Wireless and Mobile Communication*, 3-7 Dec **2018**, (Online). (E&ICT Academy IIT Guwahati & NERIST)
- **FDP** on *Recent Advances in Microprocessors, Microcontrollers, and Their Applications*, 17-21 Feb. **2015**, NERIST, Arunachal Pradesh, India. (TEQIP & NERIST)
- **FDP** on *Recent Advances in Signal Processing and Semiconductor Devices*, 24-29 Jan. **2014**, NERIST, Arunachal Pradesh, India. (TEQIP & NERIST)
- **FDP** on Integrated Circuits and Power Electronics, 30 Sept - 6 Oct. **2013**, NERIST, Arunachal Pradesh, India. (TEQIP & NERIST)
- Six days student **skill development program** on Sensor Design and Wireless Communication, 26 Sept. - 1 Oct. **2016**, NERIST, Arunachal Pradesh, India. (TEQIP, EDULIFE INDIA & NERIST)
- **Management development program** on Stress Management, 4 - 6 Nov. **2013**, NERIST, Arunachal Pradesh, India. (TEQIP & NERIST)

EXTRA-CURRICULAR ACTIVITIES

- **Group Events**

    - **First position** in TELL n SELL advertising competition (*during University Fest, NERIST*).
    - **First position** in NUKKAD NATAK drama cum awareness competition (*during University Fest, NERIST*).
    - **Second position** in Cricket (*during University Fest, NEHU*)
    - **Second position** in Badminton Men's double and Mixed double (*during University Fest, NEHU*)
    - **Second position** in Table Tennis Men's double and Mixed double (*during University Fest, NEHU*)
    - **Third position** in Volleyball (*during University Fest, NEHU*)
    - **Third position** in Skit Competition (*during University Fest, NEHU*)

- **Solo Events**

    - **Second position** in Sketching (*during University Fest, NEHU*)
    - **Second position** in Badminton Men's Single (*during Inter-Hostel Badminton Competition, NEHU*)
    - **Third position** in Arm Wrestling (*during University Fest, NEHU*)

- Many medals in *school level* games & sports, painting, athletics, debate, dancing, singing, and quiz competitions.

INTEREST AND HOBBIES

- Solving Puzzles, Playing Chess, Philately, Numismatics, Sketching, Singing, Dancing, Playing Musical Instruments.

COMPUTER SKILLS

- Well versed with business application Software like MS Word, MS Excel, MS Power-Point, Outlook, E-mail, Internet browsing etc.

REFERENCES

- **Dr. Gaurav Trivedi**, Associate Professor, EEE Deptt., IITG, Assam
  Phone No.: 9435582802, email ID: trivedi@iitg.ac.in

- **Prof. Dr. L. Joyprakash Singh**, Professor, ECE Deptt, NEHU Shillong-22, Meghalaya
  Phone No.: 9436349192, email ID: jplairen@nehu.ac.in

- **Prof. Dr. Rajesh Kumar**, Professor, NERIST, Arunachal Pradesh
  Phone No.: 9868576783, email ID: itsrk2006@gmail.com, rk@nerist.ac.in

- **Recommendations on LinkedIn** by Dr. Swanirbhar Majumder, Professor, Dept of Information Technology, Tripura University (A Central University), Agartala and Dr. Rajesh Kumar, Professor, North Eastern Regional Institute of Technology (NERIST), Under MHRD, Govt. of India.
  LinkedIn ID: dr-sarfraz-hussain-21b72118

PERSONAL DETAILS

- **Father's Name:** Prof. (Dr). M. F. HUSSAIN.
- **Date of Birth:** 6th Jan, 1989
- **Gender:** Male.
- **Marital Status:** Married.
- **Passport Status:** Valid till Oct., 2033.
- **Present Address:** School of Electronics and Communication Engineering, REVA University, Bengaluru, Karnataka - 560064, India.
- **Permanent Address:** Konal, P.O.- Sayedpur B. Toli, Dist. N/Dinajpur, West Bengal, India.
- **Nationality:** Indian.
- **Languages Known:** Mandarin, English, Hindi, Urdu, Bengali & Assamese.
- **Email-id:** sarfraz_06@ieee.org, s.hussainec@gmail.com
  Webpage: https://sites.google.com/view/sarfrazhussain/home
- **Mobile No.:** 9856433849   **Alt Mob No.:** 8787642427

DECLARATION

I hereby declare that all the information in resume are absolutely correct and I am ready to accept challenges of the future changes in the field and can work with any platforms of application.

Dated: 05-04-2025
Place: Bengaluru, India

Dr. Sarfraz Hussain