

Dr. Praveen Dwivedi



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PROFESSIONAL SUMMARY

IEEE Senior Member with over 6 years of academic and research experience in semiconductor device characterization, compact modelling, and advanced CMOS technologies at the **Department of Electrical Engineering IIT Kanpur**. Proficient in teaching, managing research projects, and publishing high-impact journals. Committed to fostering academic excellence and mentoring the next generation of engineers through cutting-edge research and innovative teaching methodologies.

Academic Qualifications

- **Ph.D., Electrical Engineering** (2014-2019)
Indian Institute of Technology (IIT), Indore
Thesis: *Influence of Transistor Architecture on the Performance of Dielectric Modulated Biosensor*
Supervisor: Prof. Abhinav Kranti
 - **M.Tech., VLSI Systems and Technology** (2012-2014)
Shiv Nadar University, (**62 NIRF ranking 2024**) Dadri, Uttar Pradesh
CGPA: 8.11/10
 - **B.E., Electronics Engineering** (2007-2011)
Madhav Institute of Technology and Science (MITS), Gwalior (Self Autonomous Government Institute)
Percentage: 70.93%
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Employment History @ Indian Institute of Technology, Kanpur

- **Project Executive Officer** (Dec 2024 – Present)-Research and academic work
 - **Research Establishment Officer (REO) Grade-I (Pay Scale-Level 11 & 7th CPC)**-Research and academic work (Dec 2019 – Dec 2024)
(I had been a regular tutor for UG courses and labs at IIT Kanpur while managing semiconductor device measurements at Nanolab. I provide modeling and measurement support to Ph.D. scholars, faculty, and industry partners **MaxLinear USA**, **Wavetek Microelectronics Taiwan**, **Tagoretech USA**, as well as **DRDO**, **ISRO**, and academic collaborators. With over 10 years of experience in TCAD-based semiconductor device modelling (Silvaco, Sentaurus), I continue to publish in top journals focused on FET devices).
 - **Institute Postdoctoral Fellow** (Sep 2019-Dec 2019)- Research and academic work
 - **Senior Project Engineer** (Dec 2018 – Sep 2019)- Research work on semiconductor device modeling
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Teaching Experience

- **Teaching Tutor**, Indian Institute of Technology, Kanpur (Jan 2020 – Present)
 - ESC201A: Introduction to Electronics (Lecture and Lab)
 - **Teaching Assistant**, Indian Institute of Technology, Indore (2014-2018)
 - Courses: Electronic Devices Lab, Analog CMOS IC Design
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Key Achievements

- Published **15+ high-impact SCI journal articles** (IEEE Trans. Electron Dev., IEEE Sens. J, Solar Energy, Physica Scripta) on advanced semiconductor device modelling and characterizations
- Google citations of more than 478 for publications
- Generated Rs. ~20 Lakhs in lab funding (2019-2024)
- Co-supervised **1 PhD, 2 M.Tech, and 1 B.Tech** student and provided support to **18 PhD students**

- Supported **research projects totalling ₹4 Crores**, showcasing an evaluation of patentability for new technologies
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Key Publications

- A. Kumar, **P. Dwivedi**, & Vivek Garg, et al., "Insights into the Potential of Sb alloyed Cu₂AgBiI₆-based Solar Cells: For Efficient Indoor Energy-Harvesting," *Solar Energy*, Jan (2025)
 - M. S. Nazir, **P. Dwivedi**, & Y. S. Chauhan et al., "Exploring Switching Behavior of Dual Gate RF GaN HEMTs", *IEEE Microwave and Wireless Technology Letters*, Dec (2024)
 - Akash Jadhav, Vivek Garg & **Praveen Dwivedi**, "Performance Assessment of Pocket Tunnel FET and Accumulation Mode FET for Detection of Streptavidin Protein" *Physica Scripta*, Sep (2023)
 - Deepak Singh, Vivek Garg, & **Praveen Dwivedi**, et al. "Comparative analysis of gate structure dependent FET based biosensors," *Materials Today Communications*, June (2023)
 - Sarita Manjhi, **Praveen Dwivedi**, & Vivek Garg et al., "Unveiling the Potential of Bismuth Oxy-Iodide (BiOI) based Photovoltaic Device for Indoor Energy Harvesting" *IEEE Transactions on Electron Devices*, Nov (2023)
 - S. S. Parihar, **P. Dwivedi** & Y. S. Chauhan et al., "Comprehensive RF Characterization and Modeling Methodology for the 5nm Technology Node FinFETs," *IEEE J. Electron Devices Soc.*, July (2023)
 - P. Dwivedi** & Y. S. Chauhan et al., "Crossing the Nernst Limit of Sensitivity in TFET-based Biosensors," *IEEE Sensors J.* Feb (2021)
 - B. S. Sengar & **P. Dwivedi** et al., "Numerical simulation: Design of high-efficiency planar p-n homojunction perovskite solar cells," *IEEE Trans. Electron Devices*, March (2021)
 - P. Dwivedi** & A. Kranti, "Dielectric modulated biosensor architecture: tunneling or accumulation-based transistor?," *IEEE Sensors J.*, April (2018)
 - P. Dwivedi** & A. Kranti, "Overcoming biomolecule location-dependent sensitivity degradation through point and line tunneling in dielectric modulated biosensors," *IEEE Sensors J.* Sep (2018)
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Research Expertise-Proficient in designing device characterization experiments that bridge academic and industrial research applications

- Semiconductor Device Characterization**: Proficient in DC IV, CV, RF-S parameters, Pulsed IV, and Noise Figure measurements.
 - Compact Modeling**: Experience with BSIM (BSIM4, BSIM-BULK) and ASM-HEMT models.
 - Device Simulation**: Expertise in TCAD tools (Silvaco, Sentaurus) for FinFET, GaN HEMT, and TFET devices.
 - Project Leadership**: Managed research projects with budgets of Rs. 3.6 Crores and supported 18 PhD students.
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Technical Skills

- Characterization Tools**: Keysight B1500A, AM3200 (Pulsed IV), PNA-X N5244 (RF Measurement)
 - Simulation Tools**: TCAD (Silvaco, Sentaurus), MATLAB, Cadence Spectre, HSPICE
 - Programming**: Python, Verilog, Verilog-A, C
 - Software**: LaTeX, MS Office, OriginPro
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Professional Service

- IEEE Senior member, and IEEE Secretary**, Electron Devices Society Uttar Pradesh Section
 - Active Reviewer**- IEEE Transactions on Electron Devices, IEEE Sensors Journal, IEDM, IEEE Journal of the Electron Devices Society, Semiconductor Science and Technology, Journal of Physics D: Applied Physics
 - Institute Representative of IIT Kanpur** for GATE 2021 Examination
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Awards & Scholarships

- MHRD Fellowship** during the Ph.D. program at IIT Indore from 2014-2019
 - Full Tuition Waiver and Scholarship** by Shiv Nadar University for two years M. Tech program from 2012-2014
 - 98 Percentile**, GATE (2011) and qualified GATE exam three times
 - Principal Engineer Technology Development job offer from **GlobalFoundries Singapore** (2022)
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References

Prof. Yogesh Singh Chauhan, Professor
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Dr. Vivek Garg, Assistant professor
Department of Electronics Engineering, SVNIT Surat
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Dr. Brajendra Singh Sengar, Assistant professor
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Email: brajendra.singh@nitsri.ac.in | Phone: +91-9179615146