MO SAJID KHAN

M.Tech (Functional Material and Devices) | IIT KHARAGPUR

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EDUCATION

Year	Degree	Institute	CGPA/Percentage
2025	M.TECH	IIT Kharagpur	7.90/10
2022	M. Sc (Electronics)	Jamia Millia Islamia	8.78/10
2018	B. Sc (Physics Mathematics)	MJP Rohilkhand	67.20 %

INTERNSHIPS

RTL INTERN | Scihubss Semiconductor Solutions Pvt. Ltd. | [Jan '25 – Present]

- Developed RTL modules and System Verilog testbenches using UVM methodology
- Performed simulation and debugging using ModelSim and Vivado
- Focused on low-power, high-performance design techniques and synthesis optimization for digital blocks

M.Tech Internship | Supervisor | Prof. Indrajit Chakrabarti | Department of E&ECE | IIT Kharagpur [May '24 - Aug '24]

- Design and Implementation of FFT/IFFT Architecture Using Verilog with Comprehensive Sanity Checks
- Developed an FFT/IFFT architecture in Verilog, optimizing for performance and efficiency in DSP applications
- Performed design verification through comprehensive simulations, ensuring functionality & reliability in signal Processing

PROJECTS

MTech Project | Dr. Vivek Dixit | Department of E&ECE | IIT Kharagpur [Aug '24 - May'25]
Title: Efficient Hardware Design of Pipelined FFT/IFFT for Digital Image Processing Applications.

- The FFT/IFFT is implemented in Verilog, enabling efficient hardware synthesis for deployment on FPGAs or ASICs
- Its pipelined nature supports real-time image processing with continuous data handling and high- speed operation
- MATLAB is used for preprocessing image data into a format compatible with the FFT module and reconverting the processed frequency-domain data back into images
- This ensures accurate functionality and seamless validation of the FFT/IFFT design

FPGA Implementation of Booth Multiplier and Brent Kung Adder| Department of E&ECE | IIT Kharagpur [Aug '24]

- Implemented an 8x8 Booth Multiplier and a 16-bit Brent Kung Adder on FPGA using Verilog
- Optimized resource usage and improved arithmetic performance for digital system applications

Design and Verification of FIFO using Verilog, Department of E&ECE | IIT Kharagpur [Sep '24]

- Designed synchronous & asynchronous FIFO using Verilog for efficient data buffering across clock domains
- Verified functionality through comprehensive testbenches and simulation workflows using Xilinx Vivado, and ensuring robust and reliable operation of the FIFO architecture

Self-Project: Sequence Detector Design Using Mealy & Moore FSMs in Verilog [Oct '24]

- Designed and implemented Mealy & Moore state machines for a sequence detector using Verilog on Xilinx Vivado
- Verified functionality through simulation, demonstrating correct detection of input sequences in both models

M.Sc. Project | S. Intekhab Amin, Assistant Professor, D/o ECE | Jamia Millia Islamia [Feb '22 – Jul '22]
Title: Design and Simulation of Ferroelectric MOS-HEMT for RF Applications

- Designed and simulated a single-gate AlGaN/GaN MOS-HEMT structure with integrated ferroelectric functionality for high-frequency RF applications using SILVACO TCAD ATLAS semiconductor device modeling tools
- Developed and incorporated a PZT (Lead Zirconium Titanate) layer beneath the gate to introduce and study ferroelectric behavior in the device
- Analyzed key characteristics such as frequency response, drain current, transconductance, and gate voltage, and plotted performance graphs using Origin software

SKILLS AND EXPERTISE

Software: MATLAB | Scilab | Silvaco TCAD ATLAS| MultiSim | LTSpice |
EDA Tools: Xilinx Vivado | ModelSim | Cadence Tools **Protocols:** I2C, SPI, AMBA, AXI
Programming Languages: Basic Python | C | Verilog HDL | System Verilog | Arduino IDE | 8085 Programming

COURSEWORK INFORMATION

Digital Electronics | VLSI Design Flow (RTL to GDS) | Analog and Circuit Electronics | Digital IC Design | Radio Frequency and Integrated Circuit | Physics of Semiconductor Devices| Static Timing Analysis |Digital Signal Processing | Technology CAD| VLSI Circuit Design & Device Modelling Principles of Quantum Devices | Computational Methods of Material Design

CERTIFICATIONS

Premium RTL Design & Verification Course | VLSI FOR ALL Pvt. Ltd | [Sep '24 – Present]
- Trained in RTL design (Verilog, FSM, CMOS) and functional verification (SystemVerilog, UVM, assertions)
- Hands-on with STA, linting, scripting (Perl, Python)

Circuit Design and SPICE Simulation – VLSI System Design (VSD) [Oct '24]
- Trained extensively in CMOS circuit design, layout principles, and simulation using SPICE-based tools such as Ngspice and eSim for both academic and project-based applications.
- Simulated a variety of basic digital and analog circuits, analyzing critical performance metrics including power consumption, propagation delay, noise margins, and signal integrity.

VLSI for Beginners | NIELIT Calicut [Jun '24]
- Learned Verilog-based RTL design and simulation using Vivado and ModelSim
- Covered basics of VLSI flow, CMOS logic, and FPGA implementation

POSITIONS OF RESPONSIBILITY

- Teaching Assistant | Physics Lab | IIT Kharagpur **[Jul '24 - Nov '24]**
- Volunteer | Photonics 2024 – 16th International Conference on Fiber Optics and Photonics
IIT Kharagpur, Department of E&ECE and Department of Physics **[Dec'24]**

Placement Coordinator at Jamia Millia Islamia **[Sep '20 - May '22]**

Physics and Mathematics Tutor | Delta Classes Jamia Nagar, DELHI
Tutored students in Physics and Mathematics for 3 years, with a focus on IIT-JEE and NEET. **[Aug'19- July'22]**

Class Representative (CR) | M.Sc | Jamia Millia Islamia [Aug '20 - May '22]
- Represented student concerns to faculty while coordinating class schedules, sharing academic updates

AWARDS AND ACHIEVEMENTS

- Qualified in **GATE (ECE) 2023** with a strong performance, demonstrating expertise in core subjects of ECE.
- Qualified **IIT JAM 2021** in Physics, showcasing proficiency in advanced undergraduate-level concepts in Physics
- Secured **3rd rank** in Jamia Millia Islamia Entrance Exam for M.Sc. Electronics (2020).
- Best Student Award, Jamia Millia Islamia University, 2022
- Best Poetry Award, Jamia Millia Islamia University, 2021
- Winner, Inter-School Physics Quiz Competition, 2015
- Participated in National Science Olympiad (NSO), qualified for Level 2, 2015

EXTRA CURRICULAR ACTIVITIES

- Volunteered for events **(Convocation '24)**, winter fest **(KHISTIZ '24)**

Hobbies: Playing Badminton, and Photography

RESEARCH EXPERIENCE & LABORATORY TRAINING

School of Nano Science and Technology (SNST), IIT Kharagpur [Sept '24 - Nov'24]
Supervisor: Prof. Dipak Kumar Goswami, Head of SNST

Research Areas: Nanoelectronics, Photonic Devices, NEMS, Nano Sensors, Nanostructured Materials & Coatings Nanobiotechnology, Computational Nanostructures

Hands-On Experience:
- Clean Room Facility operations, Dry Etching, Thermal Deposition, UV Photolithography
- Wire Bonding and UV Curing techniques

Facility Exposure: • Spark Plasma Sintering (SPS) • Electron Beam Lithography (EBL) for nanofabrication

Micro Science Laboratory, Department of Physics, IIT Kharagpur
Supervisor: Prof. Samit Kumar Ray

Measurement & Characterization Techniques:
- Electrical and Optoelectronic Measurement Units – Principles and practical applications
- X-Ray Diffractometer (XRD) – Crystallographic analysis of materials
- Atomic Force Microscopy (AFM) – Surface morphology and topological characterization
- Molecular Beam Epitaxy (MBE) – Thin-film growth in high-vacuum environments
- Thermal Deposition – Metal deposition (Au, Ag, Al)